Nano-CdS/ porous silicon heterojunction for solar cell

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Abstract— Nanostructure CdS thin film was fabricated by flash deposition technique. X-ray diffraction patterns exhibit small peaks with a hexagonal phase and the value of average grain size is about 9.603 nm. The optical transitions in nanostructure CdS film is direct transition and the value of optical energy gap is about 3.96 eV. The current-voltage characteristics of the CdS/PS solar cell under dark conditions show that forward bias current variation approximately exponentially with voltage bias. The capacitance for Nano-CdS/PS Solar Cell decreases with the increase of the reverse bias voltage and with the increasing of etching time of nPS layers, the value of built- in potential for heterojunction increases with the increasing of etching time of PS layers.

Keywords: Thin Film, Solar Cell, Heterojunctions,

1 Introduction

The II–VI semiconductor nanocrystals exhibit interesting properties and their emission spectra is very narrow (spectrally pure) and the emission colour is simply tuned by changing their size. As the nanocrystal size decreases, the energy of the first excited state decreases qualitatively following a particle-in-a-box behaviour. This size dependence and the emergence of a discrete electronic structure from a continuum of levels in the valence and conduction bands of the bulk semiconductor result from quantum confinement; hence, semiconductor nanocrystals are referred to as quantum dots) [1-4].
Cadmium sulfide (CdS), a typical one of II-VI semiconductor materials, has received considerable interest for its useful applications in solar cells, photoconductors, sensors, a buffer layer on Cu (In, Ga) Se2 (CIGS) thin films, optical detectors, field effect transistors, light emitting diodes and nonlinear integrated optical devices [5-9]. Owing to its transparency and photoconductivity, CdS thin films are also used widely as n-type window layers for thin films CdTe, CuInSe2, Cu2S and InP based heterojunction solar cells [10-12].
Porous silicon has attracted great attention due to its room temperature photoluminescence in the visible light range. As we know that, the bulk crystalline silicon has an indirect gap at 1.1 eV at room temperature, which results in a very inefficient radiative recombination and produced light in the infrared region. Therefore, the strong visible light emission in porous silicon is quite surprising and such structure can exhibit a large variety of morphologies and particles sizes. Porous silicon shows different features in comparison to the bulk silicon such as shifting of fundamental absorption edge into the short wavelength and photoluminescence in the visible region of the spectrum. However, different hypothesis is reported on photoluminescence from porous silicon surface. Porous silicon consists of a network of nanoscale sized silicon wires and voids which formed when crystalline silicon wafers are etched electrochemically in hydrofluoric acid based electrolyte solution under constant anodization conditions. The precise control of porosity and thickness allows the tailoring of optical properties of porous silicon and has opened the door to a multitude of applications in optoelectronics technology. Such structures consist of silicon particles in several nanometer size separated by voids. Hence, porous silicon layers are regarded as nanomaterials, which can be obtained by the electrochemical etching of silicon wafer. Porous silicon structures has good mechanical robustness, chemical stability and compatibility with existing silicon technology therefore has a wide area of potential applications such as waveguides, Photovoltaic is a renewable energy, which is helpful to reduce the pollution and climate change effects. Today, photovoltaic industry is dominated by silicon solar cells technology because of the reduced cost. Due to wide use of solar energy, there is the need of creation of new technologies and materials hence; porous silicon is expected to be promising one. The crystalline silicon is an important and dominant material over several years due to its well-known properties and established infrastructure for photovoltaic manufacturing. For solar cell, porous silicon layer acts as an ultra efficient anti-reflection coating, while a graded layer with varying expanded band gap offers increased absorption in visible spectrum regions. In section two, the synthesis and characterization of electrochemically anodized nanocrystalline porous silicon layers is done, then, the setup was used in fabrication as a device of Nano-CdS/PS heterojunction solar cell, and investigating the electrical properties of the heterojunction [13,14] .

2 Experimental

Crystalline silicon (C-Si) wafers (thickness 500 μm and resistivity 1.5 Ω.cm) in (400) orientation used to prepare nPS by using the Electrochemical etching process. The silicon is cleaned to remove any contamination on the surface. These pieces were rinsed with ethanol to remove dirt, followed by etching in dilute Hydrofluoric acid (10% HF) for 10 min to remove the native oxide layer. The samples rinsed with ethanol and left in environment for a few minutes to dry. The porous silicon samples were prepared by electrochemical anodic dissolution of doped p-type silicon substrates in hydroflounce acid and ethanol with platinum electrode as cathode. The electrolyte was prepared by mixing HF with concentration (40%)

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and ethanol (C2H5OH) in 1:1ratios. The porous layers on the surface of these samples were prepared at current densities of 50 mA/cm2 with various etching times (10, 20 and 30) min. Nanostructure CdS thin film was fabricated onto cleaned glass substrates with thickness 100 nm by flash deposition technique. Cleaning of substrate is important in fabrication of thin films, because it greatly influences the properties of the films deposited on it and has strong effect on the adhesion properties of the deposited films. The electrolyte was prepared by dissolving 10 mM CdSO4, 0.15 mM Na2S2O3, and 0.2 M NaOH in water. Due to the low solubility of Na2S2O3 continuous heating and stirring for several hours is required. The pH of the final electrolyte was adjusted to 3.5 with H2SO4.After preparing the nPS samples by using the Electrochemical etching process, the Nanostructure CdS thin films with thickness 100 nm were deposited on the porous silicon layers; this is achieved by using Flash evaporation technique for preparation Nano-CdS/PS heterojunction.

The crystallographic structure of films was analyzed with x-ray diffractometer (Model XRD-6000, Shimadzu, Japan) using Cu-Kα (λ=1.54Å) radiation. Diffraction patterns have been recorded over the 2θ range of 20o to 60o at the scan rate of 10o min-1.

The surface morphology and roughness of prepared samples were obtained by atomic force microscopy (Scanning probe Microscope type AA3000), supplied by Angstrom Advanced Inc. in non-contact mode. The transmission spectrums of Nanostructure CdS thin film was obtained using UV-Visible recorder spectrophotometer (Type Shimadzu- Japan), Model (UV-160) in the wavelength range (200-1100) nm. The electrical measurements for Nano-CdS/PS heterojunction, which was prepared at constant substrate temperature with different etching times of nPS layers includes current-voltage characteristic measurements in the dark and under illumination conditions by using HP-R2C unit model 4274A and 4275A multi-frequency LRC meter as well as capacitance-voltage characteristic measurements by using Keithley Digital Electrometer 616, voltmeter and D.C. power supply.

3 RESULTS AND DISCUSSION

Figure 1 shows the x-ray diffraction patterns of the CdS thin film prepared by flash evaporation technique on a glass substrate at room temperature. The x-ray diffraction patterns of the sample exhibit small peaks at 26.52° corresponding to the (002) directions. This peak corresponds to the hexagonal phase. The lattice parameter values a, and c have been calculated and are a = 4.106 Å and c = 6.637 Å which are in agreement with the JCPDS data (80-006), (JCPDS, 2000).

The presence of small peaks in the x-ray diffractogram reveals the formation of nanocrystalline CdS film. The peaks are not sharp indicating that the average crystallite size is small. Due to size effect, the peaks in the diffraction pattern broaden and their widths become large as the particles become smaller.

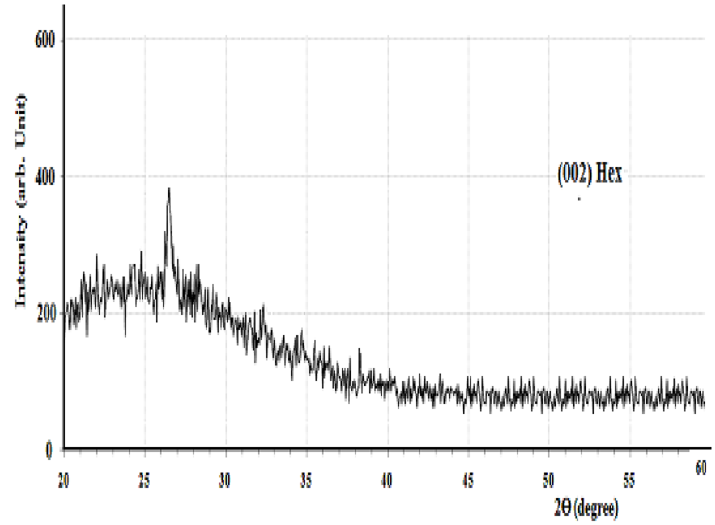


Fig.1. XRD patterns of Nanostructure CdS thin film

The optical transmission studies were carried out in the wavelength range 200 to 1100 nm. Figure 2 shows that film has high light transmission in the visible region, so CdS film, which deposited by flash evaporation of the same conditions can actively used as a window material in solar cells.

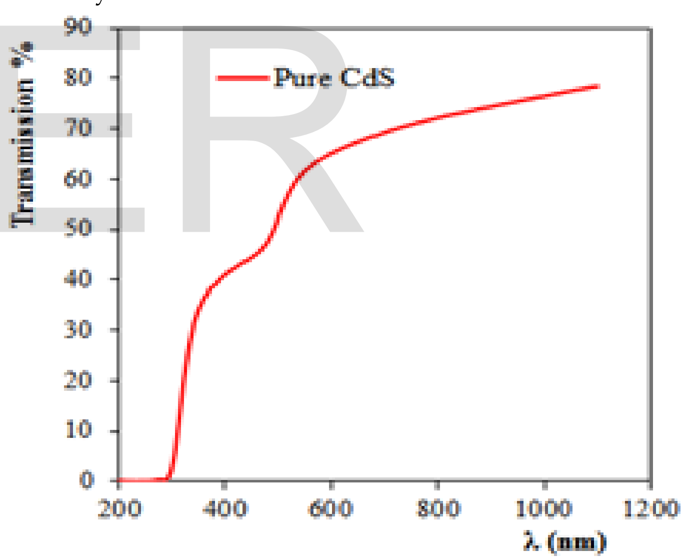


Fig. 2. Transmittance Spectra of Nanostructure CdS thin film

Optical band gap is calculated using the Tauc relation: (αhν)1/n=A(hν-Eg)

Where A is a constant and Eg is the band gap of the materials and exponent n depends on the type of transition. For direct allowed transition n=1/2. To determine the possible transitions, (αhν)2 versus hν is plotted and corresponding band gap were obtained from extrapolating the straight portion of the graph on hν axis. The direct band gap value of the sample has been obtained from (αhν)2 vs plot as shown in the Figure 3. The direct band gap value of the sample is found to be 3.96 eV, which is greater than the bulk band gap value of CdS (2.42

eV at 300 K), and this indicates the formation of nanoparticles. This value is shifted compared with the bulk value and this could be a consequence of a size quantization effect in the sample. The reduction in particle size gives a shift in the optical band gap of the sample.

The enhancement of band gap is attributed to the quantum size effect of these small crystallites, although the diameters of the nanoparticles are quite larger than the excitonic Bohr radius (~3.5 nm) of CdS. Semiconductor nanoparticles (NPs) are expected to exhibit quantum confinement effects when their size becomes comparable to the Bohr exciton radius, which results in an increase in the energy gap relative to that of the bulk solid.

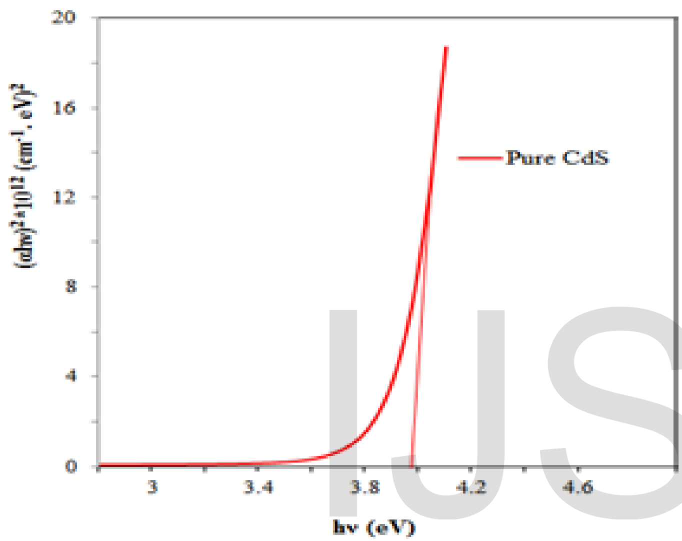
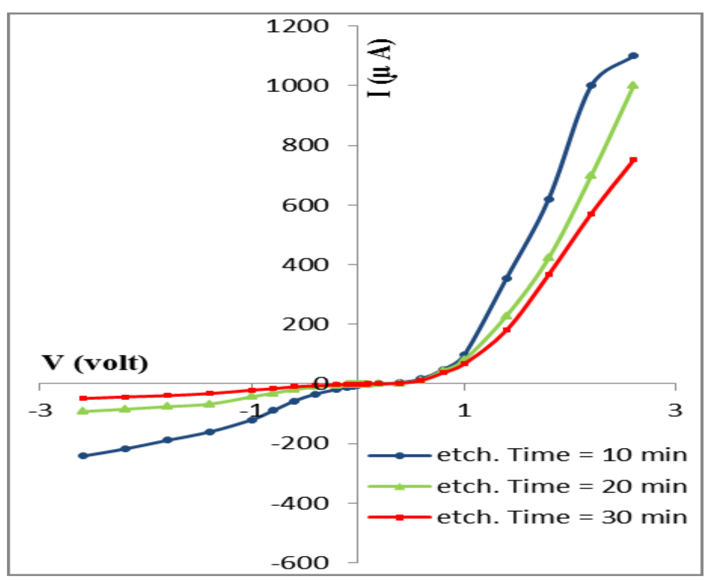


Fig. 3. A plot of (αhv)2 versus hv of Nanostructure CdS thin film

The current-voltage curves are the most commonly used characterization tool for the devices. In this technique, the current is measured as a function of voltage of the heterojunction, in both dark and light. Figure 4 represents I-V characteristics under illumination with power intensities room temperature of the Nano-CdS/PS heterojunction, containing nPS layers prepared at different etching times (10, 20 and 30) min. In general, the forward dark current is generated due to the flow of majority carriers and the applied voltage inject majority carriers which leads to decrease the value of built-in potential, and decrease the width of the depletion layer. Then majority and minority carrier concentration is higher than the intrinsic carriers concentration ($n_i < n_p$) which leads to generate recombination current at the low voltage region because that the excitation electrons from V.B to C.B will recombine with the holes which found at the V.B, and this is observed by increasing in recombination current at low voltage region. While the tunneling current is observed at high voltage region after that, there is a fast exponential increase in the current magnitude with increasing the voltage and this is called diffusion current, which is dominated. Also, the reverse bias current contains two regions in the voltage region the current increases with increasing the applied voltage, and the generation current dominates. In addition, the current-voltage characteristics exhibit rectification behavior may be due to the hetrojunction potential barrier at the CdS/PS interface.The rectification factor indicates the ratio between forward and reverse current at a certain applied bias voltage. Due to the high density of states of the nPS layer which will result in screening of internal field inside the nPS layer, this field would be nearly homogenously distributed through the nPS layer at higher voltages (V > 1 V), therefore, the forward bias characteristics will be controlled by the PSi layer resistance. This result explains the lowering of flow current in forward bias with the increasing of etching time of nPS layers, since the porosity of nPS layer increases with etching time and hence the resistance of nPS layer becomes too high which leads to low forward current. The photocurrent has been observed in reverse bias only, and we can see from this figure, that the presence of the light illumination strongly increases the reverse current. The photocurrent is always in the reverse bias direction due to it increases by increasing the depletion region width. The increasing of the reverse bias voltage leads to the increase in the internal electric field, which leads to an increasing in the probability of the separated electron-hole pairs.

The effect of preparation conditions of nPS layer such as etching time has very important effect on the photocurrent characteristics of the device, where one can observe from Figure 4, that the photocurrent is reduced with the increasing of etching time. This result can be explained since the porosity of nPS layer increases with the increasing of etching time. The increasing of porosity leads to increase the resistivity of nPS layer; therefore, the photocurrent will decrease.



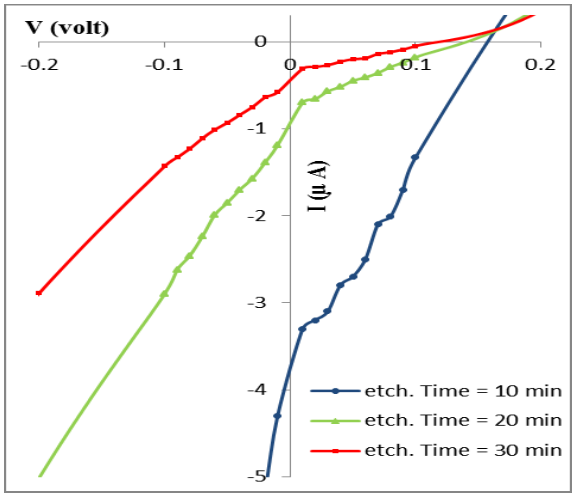


Fig. 4 I-V characteristics at dark and under illumination for Nano-CdS/PS heterojunction at forward and reverse bias voltage with different etching times of nPS layers

The capacitance-voltage characteristics have been studied in this work. The variation of capacitance as a function of reverse bias voltage in the range of (0-1) V for Nano-CdS/PS heterojunction, which prepared at different etching times (10, 20 and 30) min are shown in Figure 6. It is observed from this figure that the capacitance decreases with increasing the reverse bias. This decreasing was non-linear, that the capacitance becomes constant approximately at high voltages.

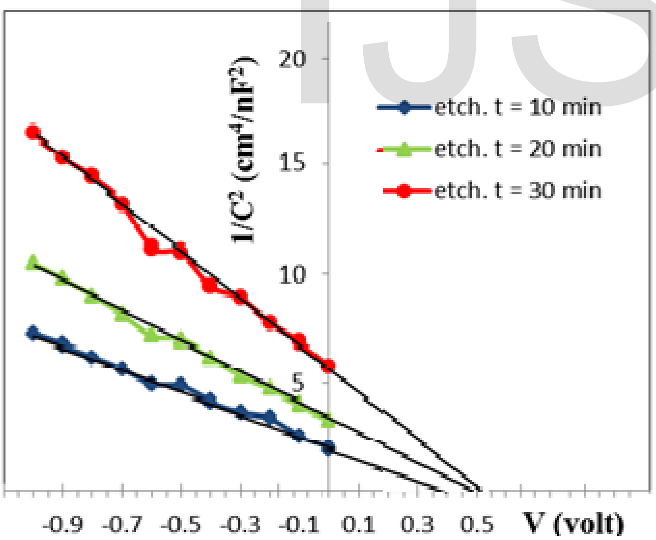


Fig. 5. The variation of $1/C^2$ as a function of reverse bias voltage for Nano-CdS/PS heterojunction with different etching times of nPS layers

This behavior is attributed to the increasing in the depletion region width which leading to the increasing of built-in voltage; it is obvious from this Figure that the capacitance at zero bias voltage (Co) decreases with the increasing of etching time of nPS layers. This is attributed to the increase of porosity with the increasing of etching time, which leads to the increasing of the depletion region width and decreasing the capacitance.

The relation between inverse capacitance squared (C^{-2}) against the reverse bias at different values of etching time are shown in Figure 6. A linear relationship between C^{-2} and reverse bias voltage was obtained for the structure, this linear relationship represents that the junction was abrupt type. The interception of the straight line with voltage axis at ($1/C^2 = 0$), represents the built-in voltage. Assuming that the resulting junction is one-sided junction, these data were calculated according to Anderson model.

Conclusion

Nanostructure CdS thin film was fabricated by flash deposition technique. X-ray diffraction patterns exhibit small peaks with a hexagonal phase and the value of average grain size is about 9.603 nm. The optical transitions in nanostructure CdS film is direct transition and the value of optical energy gap is about 3.96 eV. The current-voltage characteristics of the CdS/PS solar cell under dark conditions show that forward bias current variation approximately exponentially with voltage bias. This conforms to tunneling-recombination model, and reverse bias shows little stop and soft breakdown voltage, and the forward current decreases with the increasing of etching time. From the current-voltage characteristics under illumination, the photocurrent increases with the increasing of applied reverse bias voltage and it is reduced with the increasing of etching time. The capacitance for Nano-CdS/PS Solar Cell decreases with the increase of the reverse bias voltage and with the increasing of etching time of nPS layers, the value of built- in potential for heterojunction increases with the increasing of etching time of PS layers.

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